

*AMENDMENTS TO THE CLAIMS*

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently Amended) A time-stationary processor arranged for execution of a program, the processor comprising:

- a plurality of execution units;
- a register file accessible by the execution units;
- a communication network for coupling the execution units and the register file;
- a controller arranged for controlling the processor based on control

information derived from the program,

characterized in that at least a first execution unit and a second execution unit, of the plurality of execution units within the time-stationary processor, are arranged to produce a second identifier on validity of an output result for corresponding output ports of the first and second execution units, the processor being arranged to dynamically control writing of result data corresponding to an operation into the register file, based at least on the second identifier  
~~characterized in that the processor is further arranged to dynamically control the transfer of result data from an execution unit of the plurality of execution units to the register file, based on the control information.~~

2. (Currently Amended) A processor according to claim 1, characterized in that the control information further comprises a first identifier on the validity of ~~an~~the operation, and wherein the processor is arranged to dynamically control writing of result data corresponding to the operation into the register file, based on both the first identifier and the second identifier.

3. (Original) A processor according to claim 2, characterized in that the first identifier is delayed according to the pipeline of the corresponding execution unit arranged for executing the operation.

4. Canceled.

5. (Currently Amended) A processor according to claim 34, characterized in that the processor is further arranged to dynamically control writing of result data corresponding to the operation into the register file, based on the first identifier, the second identifier and an input datum.

6. (Original) A processor according to claim 1, characterized in that the register file is a distributed register file.

7. (Original) A processor according to claim 1, characterized in that the communication network is a partially connected communication network.

8. (Currently Amended) A method for controlling a time-stationary processor arranged for execution of a program, wherein the processor comprises:

- a plurality of execution units;
- a register file accessible by the execution units;
- a communication network for coupling the execution units and the register file;

- a controller arranged for controlling the processor based on control information derived from the program,

characterized in that the method for controlling the time-stationary processor comprises the steps of:

producing, by a first execution unit and a second execution unit of the plurality of execution units within the time-stationary processor, a second identifier on the validity of an output result for a corresponding output port of the execution unit, and dynamically controlling the writing of result data corresponding to an operation into the register file, based at least on the second identifier.

~~dynamically controlling the transfer of result data from an execution unit of the plurality of execution units to the register file, using the control information.~~

9. (New) The method of claim 8, characterized in that the control information further comprises a first identifier on the validity of the operation, and wherein the processor carries out the step of dynamically controlling the writing of result data corresponding to the operation into the register file, based on both the first identifier and the second identifier.

10. (New) The method of claim 9, characterized in that the first identifier is delayed according to the pipeline of the corresponding execution unit arranged for executing the operation.

11. (New) The method of claim 10, characterized in that the processor is further arranged to dynamically control writing of result data corresponding to the operation into the register file, based on the first identifier, the second identifier and an input datum.

12. (New) The method of claim 8, characterized in that the register file is a distributed register file.

13. (New) The method of claim 8, characterized in that the communication network is a partially connected communication network.